WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor device, comprising:

providing a substrate;

forming a gate structure on said substrate, said gate structure including a gate dielectric layer on said substrate and a gate conductive layer on said gate dielectric layer;

forming an oxide layer conformally covering said substrate and said gate structure;

forming a dielectric layer covering said oxide layer;

removing a portion of said dielectric layer to form a spacer on a sidewall of said gate structure until said oxide layer is exposed, said oxide layer disposed between said spacer and said gate structure being deemed as an oxide spacer;

performing an oxygen plasma treatment process to form an silicon oxide layer in said substrate below said oxide layer, said silicon oxide layer and said oxide layer constituting an offset oxide layer; and

forming a source/drain region in said substrate at two sides of said gate structure.

2. The method of claim 1, wherein a material of said oxide layer includes silicon oxide.

3. The method of claim 1, wherein a material of said dielectric layer includes silicon nitride.

4. The method of claim 1, wherein a width of said oxide spacer is not larger than a width of said spacer.

5. The method of claim 1, wherein said step of removing a portion of

said dielectric layer includes performing an anisotropic etching process.

6. The method of claim 5, wherein said anisotropic etching process is a reactive ion etching process.

7. The method of claim 1, wherein said oxide layer has an etching selectivity relative to said dielectric layer for said step of removing a portion of said dielectric layer.

8. The method of claim 1, before said step of forming said oxide layer, further comprising forming a source/drain extension region in said substrate at two sides of said gate structure.

9. A semiconductor device, comprising:

a substrate;

a gate structure on said substrate, said gate structure including a gate dielectric layer on said substrate and a gate conductive layer on said gate dielectric layer;

an oxide spacer on a sidewall of said gate structure;

a spacer on said oxide spacer;

a source/drain region in said substrate besides said gate structure and said spacer; and

an offset oxide layer on said substrate and said source/drain region, said offset oxide layer having a bottom surface below a bottom surface of said gate dielectric layer.

10. The device of claim 9, wherein a material of said oxide spacer includes silicon oxide.

11. The device of claim 9, wherein a material said spacer includes

silicon nitride.

12. The device of claim 9, wherein said oxide spacer has an etching selectivity relative to said spacer.

13. The device of claim 9, further comprising a source/drain extension region below said oxide spacer and adjacent to said source/drain region.

14. The device of claim 9, wherein a width of said oxide spacer is not larger than a width of said spacer.